REMARKS

Claims 6-8, 10 and 11 remain pending in the application. Claims 19-24 are newly added to the application. Reconsideration and allowance of the application is requested.

As can be seen the above amendment, claims 12 and 13 are canceled with claim 6 being amended to substantially incorporate the limitations of claim 13. In this regard, claim 6 is substantively claim 13, previously considered, and this amended should be entered. New claims 19-24 though different in scope than the previously pending claims, are still drawn to closely related subject matter, and are thus believed to be properly presented. New claims 19-24 do not add any new matter, and entry is respectfully requested.

Applicant asserts that the cited references, i.e., Lee et al., Ishida et al., and Cunningham et al., cited in the action neither teach nor suggest a method for fabricating a CMOS image sensor as claimed. For example, claims 6 and 19 require, among other things, a) providing a semiconductor structure, wherein the semiconductor structure includes an N-type impurity region and a gate electrode, b) forming a first spacer on a first sidewall of the gate electrode and a fourth spacer on a second sidewall of the gate electrode, wherein the first spacer is overlapped with a portion of the N-type impurity region, c) removing the fourth spacer by a photo resist pattern covering the impurity region and the first spacer, d) forming a second spacer on a sidewall of the first spacer and a third spacer on a the second sidewall of the gate electrode after removing the fourth spacer, e) carrying an ion implantation to form a P-type impurity region on the impurity region to thereby obtain a photodiode, and f) forming a floating diffusion region spaced away from the impurity region by a predetermined distance.

Particularly, Lee et al. and Ishida et al. show plural spacers formed on the sidewalls of the gate structure. However, Lee et al. do not describe removing any spacer among spacers 680 and 682 formed on the sidewalls of gate structure. Ishida et al. do not teach forming a spacer on the sidewall of the spacer already formed on one sidewall of the gate structure after removing a spacer formed on the other sidewall of the gate structure.

Thus, neither Lee et al. nor Ishida et al. teach or suggest each and every limitation of the claims as required to render the claims anticipated or unpatentable.

Furthermore, Ishida et al. show forming an inner spacer 13 and an outer spacer 14 on both sidewalls of the gate electrode and removing the outer spacer 14 formed on one sidewall of the gate electrode. As compared with an embodiment of the claimed invention, the Ishida et al process is more complicated as removing the outer spacer 14 formed on one of the sidewalls of the gate electrode according to Ishida et al. should be performed based on HF etch rates of inner and outer spacers. As a result, the inner spacer 13 should have different characteristic for dilute aqueous HF as compared with the outer spacer 14.

According to an embodiment of the claimed invention, the second spacer pair is formed after removal of one spacer of the first spacer pair. Thus, regardless of the physical or chemical characteristics of the first or second spacer pairs, it is a simple process to form the gate electrode having different width spacers formed on both sidewalls. Accordingly, using a process according to an embodiment of the claimed invention it is easier and more convenient to fabricate a gate structure in a CMOS image sensor than the process of either Lee et al. or Ishida et al.

Accordingly, Applicant believes that all claims according to above amendment are now allowable, and such action is respectfully requested.

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Respectfully submitted,

Electronic signature: /Anthony G. Sitko/
Anthony G. Sitko
Registration No.: 36,278
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive, Suite 6300
Sears Tower
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant